1. Choose the correct answer for the following questions. (40%)

(1) An amplifier has that open voltage gain of +40dB, input resistance of 10KΩ and output resistance of 100Ω, and is used to drive 1 KΩ load. Find the power gain in dB. (A)40 (B)49 (C)80 (D)98 (E)102

(2) For the ideal opa circuit shown in Fig.1 and R_1 = 1kΩ, R_2 = 25kΩ, R = 10kΩ, find the input resistance R_i in Ω. (A)1k (B)10k (C)25k (D)26k (E)∞

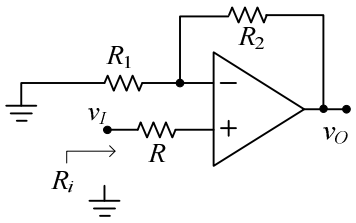

Fig.1

(3) Actually, the tuned amplifier is a (A)High Pass Filter (B)Band Pass Filter (C)Low Pass Filter (D)Notch Filter (E)All Pass Filter.

(4) For the ideal opa circuit shown in Fig.2 and if the op amp has ±12V output saturation levels, R_1 =10kΩ, R_2 = 40kΩ**.** Which is the possible input voltage v_I such that the output voltage will transform from -12V to +12V? (A)-4V (B)-2V (C)0V (D)2V (E)4V

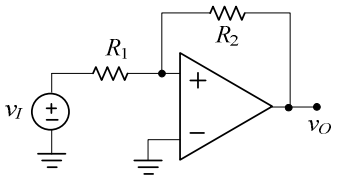

Fig.2

(5) Decide the locations of the zeros from the circuit in Fig.3 and derive that the circuit is a (A)High Pass Filter (B)Band Pass Filter (C) Low Pass Filter (D)Notch Filter (E)All Pass Filter.

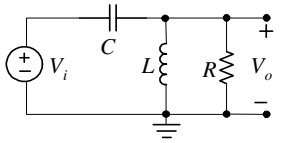

Fig.3

(6) A STC network has the following transfer function:

$$T(s)=\frac{V_o(s)}{V_i(s)}=\frac{100}{s+1}$$

Which statement is correct about this network?

(A)Corner Frequency: 100 rad/sec

(B)voltage gain: 100 dB at frequency ω = 1 rad/sec

(C)dc gain: 40dB

(D)high frequency gain: 100

(E)If the frequency is larger than the Corner Frequency, the gain decreases 10dB while the frequency increases 10 times.

(7) Which amplifier will be on the last stage of multistage amplifier for the consideration of impedance? (A)Common Emitter (B)Common Base (C)Common Collector (D)Common Gate (E)Common Source

(8) The circuit shown in Fig.4 is a NMOS digital switch under that gate voltage $V_G = V_{DD} = 5$V, the FET with $V_t = 1$V, and the capacitor C is the output load capacitance. The v_I is the input voltage, and v_O is the final output voltage. Which statement in the following is correct? (A)if $v_I = 5$V, then $v_O = 5$V (B)if $v_I = 5$V, then $v_O = 0$V (C)if $v_I = 0$V, then $v_O = 0$V (D)if $v_I = 0$V, then $v_O = 5$V (E)if $v_I = 2.5$V, then $v_O = 2.5$V

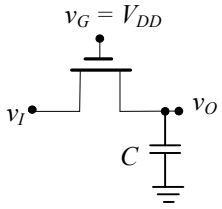

Fig.4

(9) For the circuit shown in Fig.5, please indicate the resistor that supports the negative feedback for bias. (A)R_1 (B)R_2 (C)R_C (D)R_E (E)both R_1 and R_2

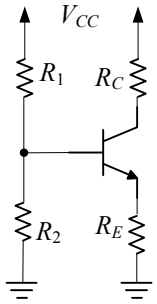

Fig.5

(10) Which parameters in the following are correct for the normal digital circuits operations?
(A)$V_{OH} = 3.2$V, $V_{IH} = 1.8$V, $V_{OL} = 0.3$V, $V_{IL} = 0.8$V
(B)$V_{OH} = 1.8$V, $V_{IH} = 3.2$V, $V_{OL} = 0.3$V, $V_{IL} = 0.8$V
(C)$V_{OH} = 1.8$V, $V_{IH} = 3.2$V, $V_{OL} = 0.8$V, $V_{IL} = 0.3$V
(D)$V_{OH} = 3.2$V, $V_{IH} = 1.8$V, $V_{OL} = 0.8$V, $V_{IL} = 0.3$V
(E)$V_{OH} = 2.8$V, $V_{IH} = 3.2$V, $V_{OL} = 0.5$V, $V_{IL} = 1.0$V

2. Consider the circuit shown in the Fig.6 with $R = 1$KΩ. Assume the diode have a 0.7V voltage drop at 1 mA current and $n = 2$. The power supply voltage V^+ has a dc value of 12V on which is superimposed a 60Hz sinusoid of 1V peak amplitude. Calculate
(a)the dc voltage drop of the diode V_D by the iteration (three significant figures), and
(b)the amplitude of the sine-wave signal $\hat{v}_d$ appearing across the diode. (10%)

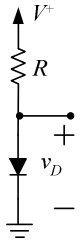

Fig.6

3. The circuit as Fig.7 shows and the transistor has $V_t = 1$V, $k_n'(W/L) = 0.25$mA/V^2, $V_A = 50$V. If $V_{DD} = 12$V, $R_D = 10$KΩ, $R_G = 10$MΩ, $R_L = 10$KΩ, find
(a)DC drain current I_D (5%)
(b)voltage gain. (5%)
(c)input resistance R_{in}. (5%)
(d)the largest allowable input signal. (5%)

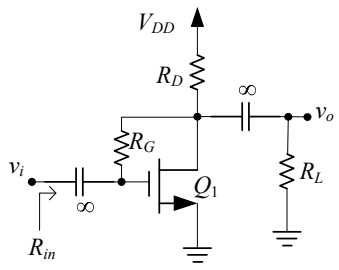

Fig. 7

4. For the circuit shown in Fig.8 under that V_{CC} = +12V, R_C = 6KΩ, R_E = 3KΩ, find the highest voltage to which the base can be raised while the transistor remains in the active mode. Assume $\alpha \approx 1$. (10%)

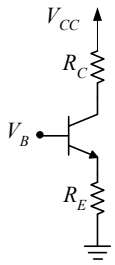

Fig.8

5. An active-loaded MOS differential amplifier as shown in Fig.9 is specified as follows: $(W/L)_n$ = 100, $(W/L)_p$ = 60, $\mu_n C_{ox} = 2\mu_p C_{ox}$ = 0.2 mA/V^2, I = 20μA, $|V_{An}| = |V_{Ap}|$ = 10V. If the differential input voltage $v_{id} = v_{G1} - v_{G2}$, calculate differential voltage gain $A_d = v_o/v_{id}$. (10%)

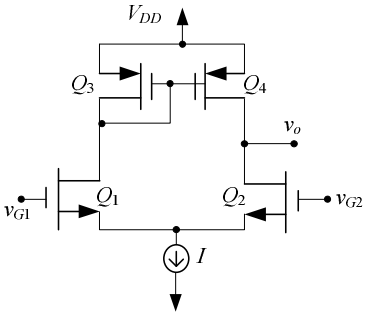

Fig.9

6. For the oscillator shown in Fig.10, please use the oscillation principle to derive
(a)the frequency of oscillation (b)R_2/R_1 for oscillation. (10%)

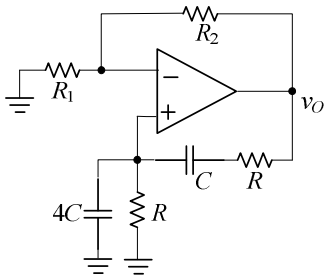

Fig. 10