(1) EXPLAIN or DESCRIBE the following key terms:

(a) LED (5%)
(b) Schottky diode (5%)
(c) CMOS (5%)
(d) Early Voltage (5%)
(e) Threshold voltage (5%)
(f) Depletion mode (5%)
(g) Corner frequency (3 dB frequency) (5%)
(h) Virtual ground (5%)

(2) For the circuit shown in the **Figure 1**, the transistor parameters are $\beta_0 = 99$ and $r_0 = \infty$. (a) Determine the q-point values. (*i.e.*, the values of I_{CQ} and V_{CEQ}). (b) **FIND** the small-signal hybrid-π parameters. (*i.e.*, the values of g_m and r_π). (c) **FIND** the small-signal voltage gain $A_v = v_o/v_s$. (20%)

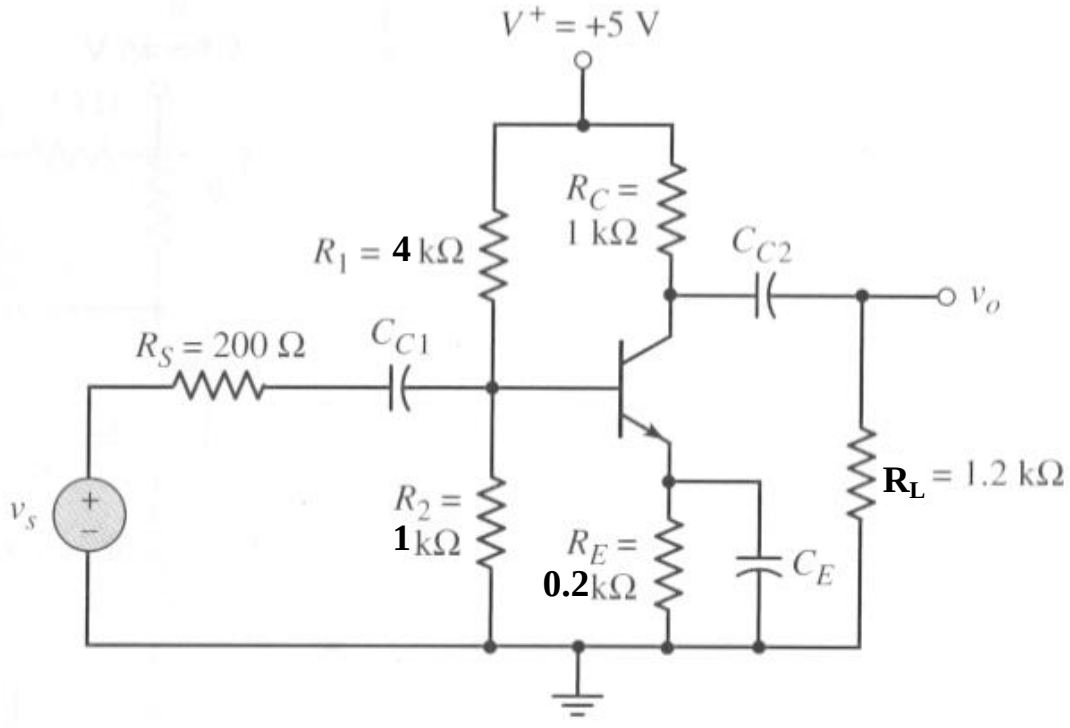

Fig. 1

(3) **FIND** the logic function implemented by the circuit shown in the **Figure 2**. (10%)..

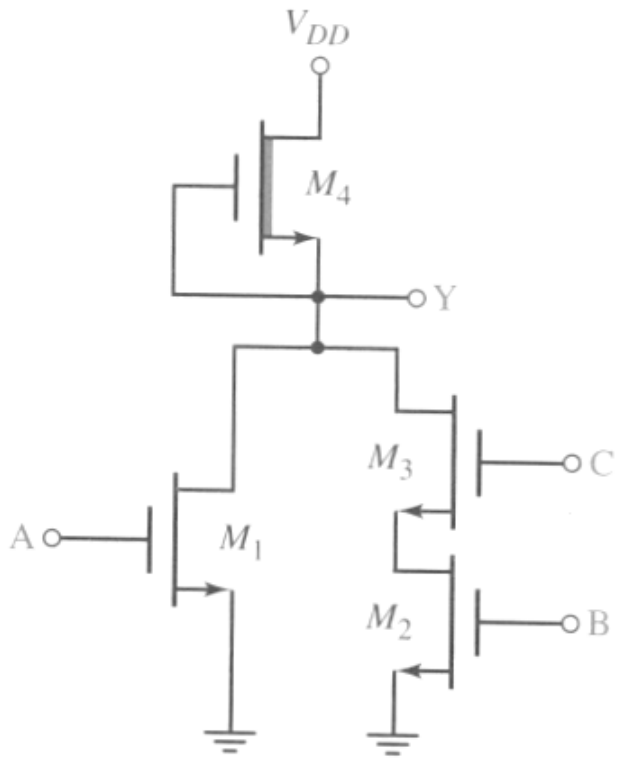

Fig. 2

(4) A high-frequency bipolar transistor is biased at $\boldsymbol{I_{CQ}}$ = 0.75 mA and has parameters C_μ = 0.15 pF, f_T = 7.5 GHz, and β_0 = 250. **Determine** C_π and f_β (10%).

(5) **Calculate** $\boldsymbol{V_{bi}}$ in a silicon pn junctions at T = 300 ^oK for: (a) $\boldsymbol{N_d} = \boldsymbol{N_a} = 10^{15}$ cm $^{-3}$; (b) $\boldsymbol{N_d} = \boldsymbol{N_a} = 10^{18}$ cm $^{-3}$.(For silicon, $\boldsymbol{n_i} = 1.5 \times 10^{10}$ cm $^{-3}$). (10%)

(6) For each circuit shown in Fig. 3, **find** the voltage gain and the input resistance. Assuming all op amps are ideal. (10%)

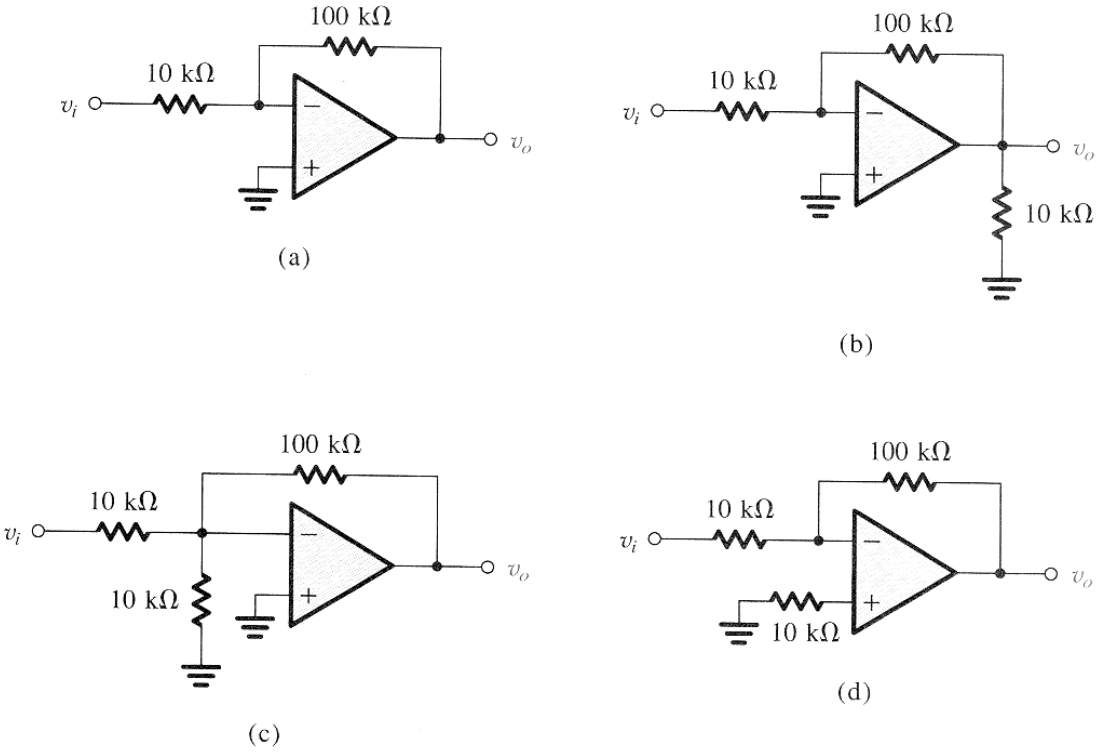

Fig. 3