1.(21%) Explain the following terminologies:

    1) (3%) Direct Memory Access (DMA)

    2) (3%) Associative Memory

    3) (3%) Von Neumann Bottleneck

    4) (3%) Nonvolatile Memory

    5) (3%) MIMD Machines

    6) (3%) Denial of Service

    7) (3%) IP Spoofing

2. (15%) Given the pattern 1001, what does it represent? Assuming

    1) (3%) It's a one's complement integer.

    2) (3%) It's a two's complement integer.

    3) (3%) It's an unsigned integer.

    4) (3%) It's a BCD code.

    5) (3%) It's a Excess-3 code

    Write down your answer in decimal format.

3. (12%) Show the multiplication 3×-7 using Booth's algorithm. A, B, C and D are 4-bit registers which can perform shift left and shift right operations.   Initially, 3 is stored in A, -7 is stored in B. The product will be stored in registers C and D. Show, step by step, the contents of C and D after each shift operation is performed.
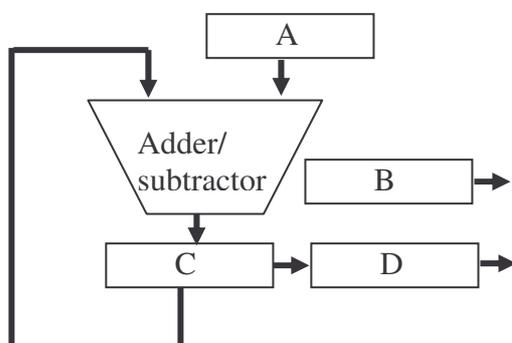
	C	D
Initial	0000	0000
After 1st shift		
After 2nd shift		
After 3rd shift		
After 4th shift		

4. (16%) A non-pipelined circuit C0 is designed to perform an arithmetic operation on a pair of numbers as shown in Figure 1. A pipelined circuit which performs the same operation on a pair of numbers is shown in Figure 2. In the figures, r0, r1, r2 and r3 are registers. s1, s2 and s3 are circuit segments for performing parts of the operation. The propagation delays of the circuits are given as follows: r0=r1=r2=r3=20ns; C0=200ns; s1=100ns; s2=40ns; s3=60ns. Answer the following questions. You can make any reasonable assumption if necessary.

1) (4%) What is the minimal time for the non-pipelined circuit to complete the operations on 100 pairs of numbers?

2) (4%) What is the minimal time for the pipelined circuit to complete the operations on 100 pairs of numbers?

3) (4%) What is the minimal number of pairs for the pipelined circuit to achieve speedup equal to 1.6?

4) (4%) What is the maximum speedup that the pipelined circuit can achieve?
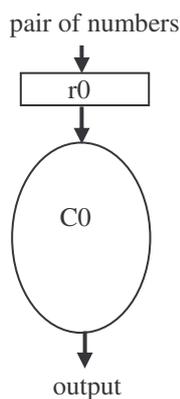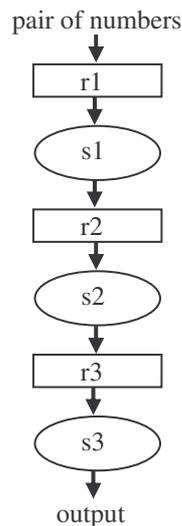
Figure 1   Figure 2

5. (16%) Design the following devices based on OR gates, AND gates, or INVERTER.
   1) (6%) Full adder
   2) (4%) 2×1 multiplexer
   3) (6%) Use the modules developed in 1) and any necessary gates to implement a 4-bit 2's complement adder/subtractor.

6. (10%) Suppose the procedure modify is defined by

> Procedure **Modify**(Y)
> Y←X+9;
> print the value of X;
> print the value of Y;.

Also suppose that X is a global variable.

1) (5%) If parameters are passed by value, what will be printed when the following program segment is executed?

> **Main** program
> X←5;
> print value of X;
> apply the procedure **Modify** to X;
> print value of X;

2) (5%) What if parameters are passed by reference?

7. (10 %) Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache. Assume a main memory access time is 300 cycles, including the entire miss handling. Suppose the miss rate per instruction at the primary cache is 3%.Which of the following secondary caches you should use such that CPI will be no more than 5.5?

cache parameters	secondary cache A	secondary cache B	secondary cache C
miss rate to main memory	0.5%	1%	1.5%
cache access time	120 cycles	40 cycles	10 cycles