1. For the circuit in Fig. 1, the NMOS and PMOS transistors are matched with $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1\ mA/V^2$ and $V_{tn} = -V_{tp} = 1V$. Assume $\lambda = 0$ for both devices, find the drain current i_{dn} and the voltage v_o for
   (a) $v_i = 0$ V. (10%)
   (b) $v_i = 2.5$ V. (10%)

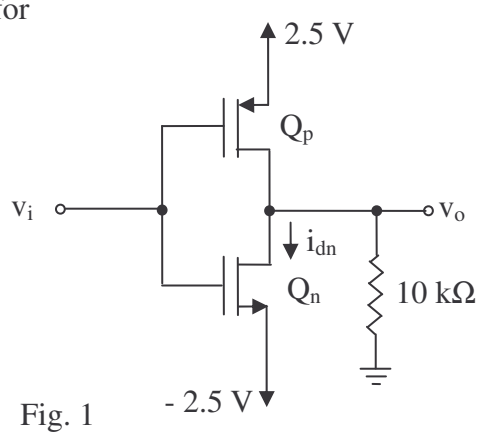

Fig. 1

2. To design a difference amplifier shown in Fig. 2, we will need to select the resistors properly.
   (a) Find the value of R4 such that the common-mode gain is 0. (10%)
   (b) Use the same R4 from (a) and find the differential gain. (5%)

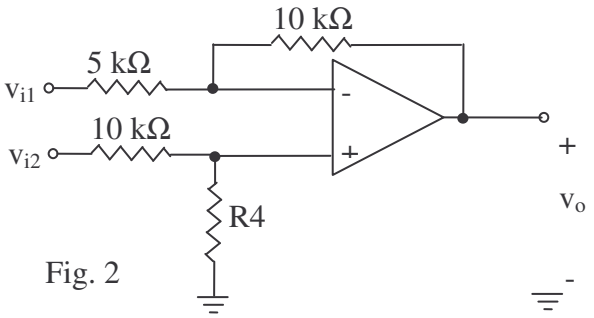

Fig. 2

3. Find the voltage gain (v_o/v_i) of the transistor amplifier shown in Fig. 3 for the small-signal operation. Assume $\beta = 100$. Hint: use the hybrid-π model to represent the BJT as a voltage-controlled current source. (15%)

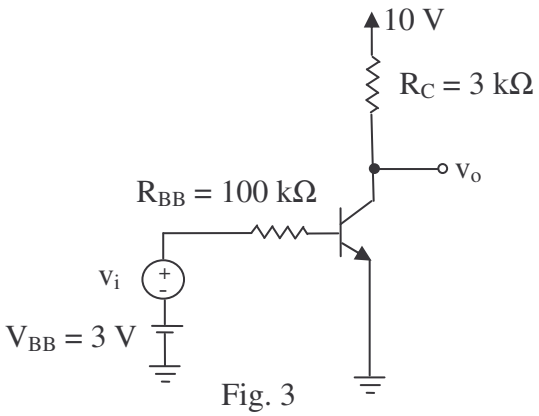

Fig. 3

4. Assume that for the basic CMOS inverter $(W/L)_n = n = 2$, $(W/L)_p = p = 5$ and that channel length is 0.25μm. For the circuit shown in Fig. 4, find (a) the relation between the output Y and the input signal A, B, C, D (b) (W/L) ratio for each transistor.
(20%)

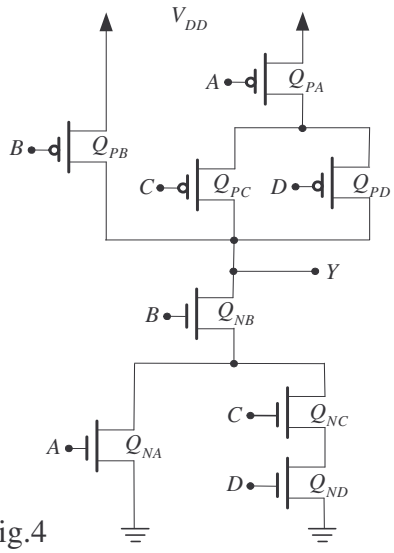

Fig.4

5. For the ideal op amp circuit in Fig.5, (a) what is the circuit? (b) please derive the relation between the v_I and v_O (c) plot the voltage transfer characteristic of the circuit (d) Assume that the op amp has ± 12V output saturation levels, R_1 =10 KΩ, R_2 = 40 KΩ and v_I = -5V, then the voltage of v_O =?
(20%)

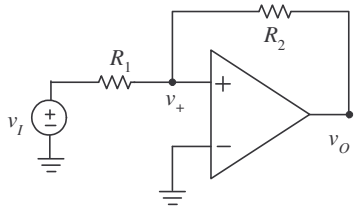

Fig.5

6. A multi-pole amplifier has a first pole at 1MHz, second pole at 10MHz and an open-loop gain of 100dB. This amplifier is to be compensated for closed-loop gain as low as 20dB. If the compensation is obtained by moving the first pole, at what frequency must the first new pole be placed?
(10%)