1. For the circuit in Fig. 1, the NMOS transistor Q_1 has $V_t = 1V$, and $\mu_n C_{ox} = 20\mu A/V^2$, and the PMOS transistor Q_2 has $V_t = -1V$, and $\mu_p C_{ox} = 10\mu A/V^2$. Given $(W/L)_1 = 2(W/L)_2$. Find the value of V_m. (20%)

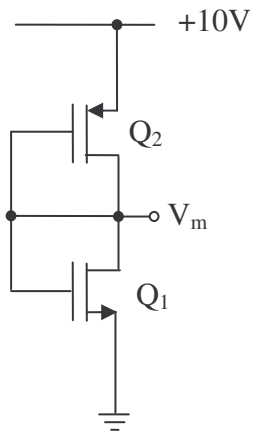

Fig. 1

2. Assume the op amp in Fig. 2 to be ideal. Find v_o in terms of the input voltages v_1, v_2 and v_3. Hint: use superposition. (10%)

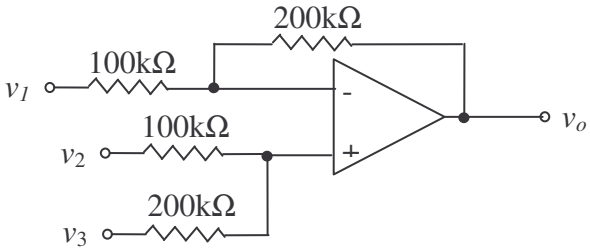

Fig. 2

3. For the circuit in Fig. 3, the *npn* transistor Q_1 has $V_{BE} = 0.7V$ and the *pnp* transistor Q_2 has $V_{EB} = 0.7V$. Find the values of V_o for:
   (a) $\beta = \infty$. (10%)
   (b) $\beta = 100$. (10%)

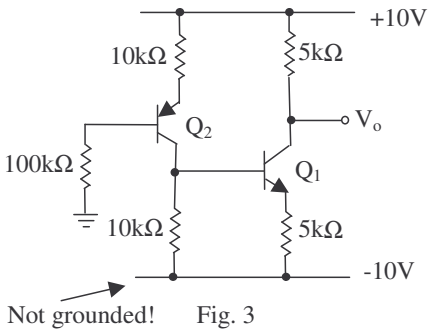

Fig. 3

4. Consider the cascode configuration of the differential amplifier shown in Fig. 4. Find the output resistance and the voltage gain of the circuit. (negligible body effect) (10%)

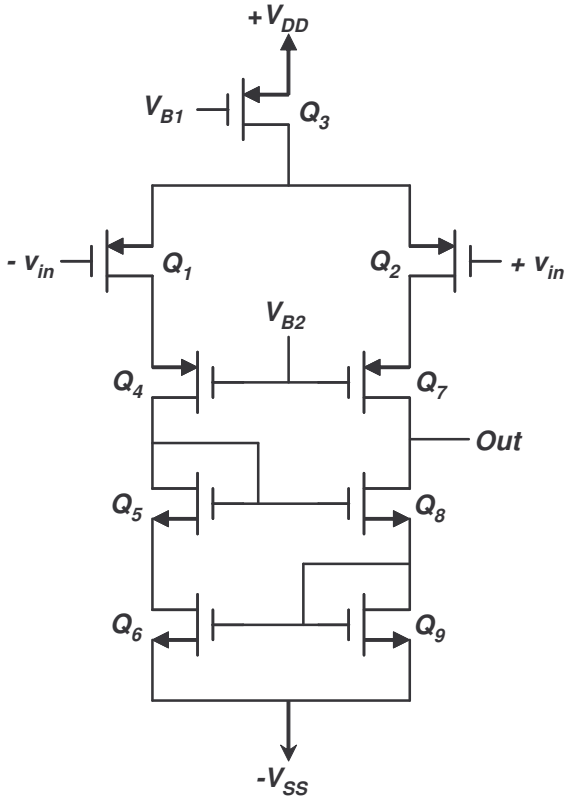

Fig. 4.

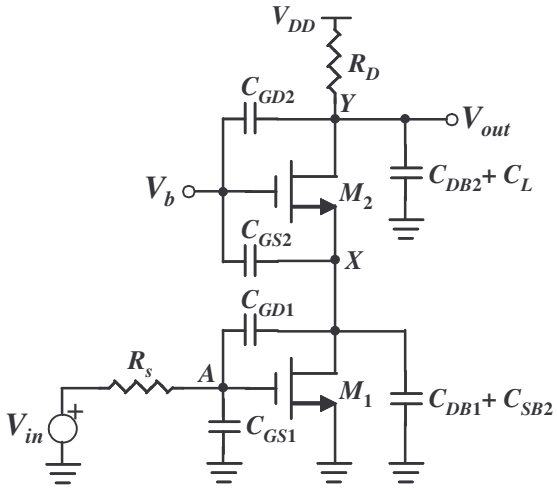

Fig. 5.

5. Consider the circuit shown in Fig. 5. Find the approximate poles of the three nodes *A*, *X*, and *Y*. (negligible channel-length modulation) (20%)

6. Find the closed-loop gain and the output impedance of the circuit shown in Fig. 6. (20%)

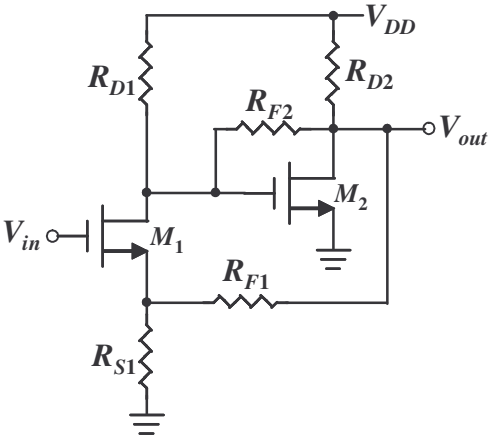

Fig. 6.