國　　立　　宜　　蘭　　大　　學

１０８學年度研究所碩士班考試入學

電子學(範圍相當於 Sedra/Smith 微電子學前七章)試題

（電子工程學系碩士班）

准考證號碼：

《作答注意事項》

1.請先檢查准考證號碼、座位號碼及答案卷號碼是否相符。

2.考試時間：100 分鐘。

3.本試卷共有 6 題，第 1 題為 10 個單選題，每題 4 分，小計 40 分；第 2~6 題為非選擇題，小計 60 分，合計 100 分。

4.請將答案寫在答案卷上。

5.考試中禁止使用手機或其他通信設備。

6.考試後，請將試題卷及答案卷一併繳交。

7.本試卷採雙面影印，請勿漏答。

8.本考科可使用非程式型（不具備儲存程式功能）之電子計算機。

1. Choose the correct answer for the following questions. (40%)

(1) A STC network has the transfer function: $T(s)=\dfrac{s}{s+100}$.
At frequency ω = 100 rad/sec, the phase of $T(s)$ is (A) –90° (B) –45° (C) 45° (D) 90°.

(2) Which is NOT correct for the property of ideal op amp?
(A) open loop gain: ∞ (B) input current: 0
(C) input resistance: 0 (D) CMRR: ∞

(3) An opa non-inverting amplifier with the opa with f_t = 1 MHz. Find its 3 dB frequency of closed-loop amplifier with gain of 100.
(A) 100 kHz (B) 10k Hz (C) 1 kHz (D) 100 Hz

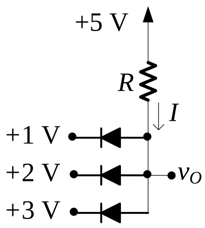


Fig. 1.(3)

(4) For the ideal diode circuit shown in Fig. 1.(3) and assume R = 1 kΩ. Then the current I =?
(A) 4 mA (B) 3 mA (C) 2 mA (D) 1 mA

(5) The temperature coefficient (TC) of the general diode is
(A) 1 mV/°C (B) 2 mV/°C (C) –1 mV/°C (D) –2 mV/°C

(6) Which is correct about the Common Collector amplifier?
(A) for voltage amplification (B) high input resistance
(C) high voltage gain (D) high output resistance

(7) In Fig. 1.(6), which is correct about the current gain of BJT in saturation region β_{forced} and that β in active region?
(A) $\beta = I_E / I_C$ (B) $\beta_{\text{forced}} < \beta$
(C) $\beta_{\text{forced}} = \beta$ (D) $\beta_{\text{forced}} > \beta$

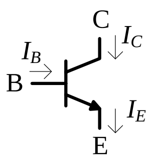


Fig. 1.(6)

(8) The resistance r_e of BJT is defined as:

(A) $\dfrac{v_{ce}}{i_e}$ (B) $\dfrac{v_{ce}}{i_b}$ (C) $\dfrac{v_{be}}{i_b}$ (D) $\dfrac{v_{be}}{i_e}$

(9) An enhancement-type PMOS FET, with V_{tp} = –1 V, has its source terminal voltage = 4.0 V and a 2 V dc applied to the gate. What region does the device operate for V_D = 3.5 V?
(A) Saturation (B) Cutoff (C) Triode (D) Active region.

(10) What is correct about folded cascode shown as the Fig. 1.(10)?
(A) output resistance is larger and output DC voltage is reduced
(B) output resistance is smaller and output DC voltage is increased
(C)output resistance is larger and output DC voltage is increased
(D) output resistance is smaller and output DC voltage is reduced

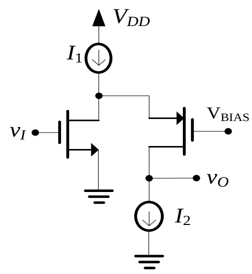
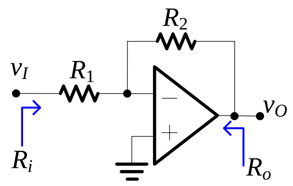
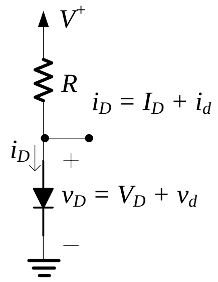


Fig. 1.(10)

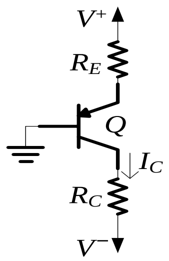
2. For the circuit with $R_1 = 2$ kΩ, $R_2 = 20$ kΩ, assume the opa is ideal, and find
(a) closed loop gain $G = v_O/v_I$
(b) input resistance R_i
(c) output resistance R_o.
(d) If the open loop gain of the opa is $A = 10^3$. Find closed loop gain $G = v_O/v_I$.
(20%)



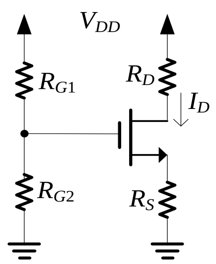
3. Consider the circuit shown in the figure with $R = 1$ kΩ and the power supply voltage V^+ has a dc value of 8 V. Assume the diode has a current 1 mA at a voltage drop 0.7 V. Calculate
(a) the dc voltage drop of the diode V_D and current I_D by the iteration (three significant figures).
(b) If V^+ is superimposed a 60 Hz sinusoid of 1 V peak amplitude, find the amplitude of the sine-wave signal $\hat{v}_d$ appearing across the diode.
(10%)



4. Assume $V^+ = +10$ V, $V^- = -10$ V, $R_C = 2$ kΩ, $R_E = 5$ kΩ and BJT's $\beta = 100$.
(a) Find the current I_C.
(b) Find the largest value to which R_C can be raised while the transistor remains in the active mode.
(10%)



5. For the circuit shown in figure, let $V_{DD} = 8$ V, $R_{G1} = R_{G2} = 2$ MΩ, $R_D = 4$ kΩ, $R_S = 3$ kΩ. The transistor has $V_t = 1$ V, $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect. Find drain current I_D.
(10%)



6. The cascode amplifier shown in the circuit is operated at a current of 0.2 mA with all devices operating at $|V_{OV}| = 0.2$ V. All devices are matched and have $|V_A| = 2$ V. Find
(a) output resistance R_o (b) voltage gain A_v.
(10%)