1. (a) For a voltage amplifier, what are its ideal input resistance and ideal output resistance? (5%)

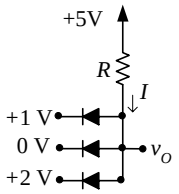

Fig. 1

(b) For the ideal diode circuit shown in the Fig. 1, find current I. Assume R = 1KΩ. (5%)

(c) Describe the reason that causes the potential barrier in the depletion region of *pn* junction. (5%)

(d) Please draw a figure of drain current i_D vs. v_{GS} for both Enhancement mode NMOS and Depletion mode NMOS. (5%)

(e) Compared with common-gate amplifier and common-drain amplifier, what's the main reason that limits the high frequency response of the common-source amplifier? (5%)

(f) For the circuit shown in Fig. 2, if $R_2 = 2R_1$ and v_I = -2V, indicate the voltages of v_O and v_A. Assume that the diodes have 0.7V voltage drops when conducting. (5%)

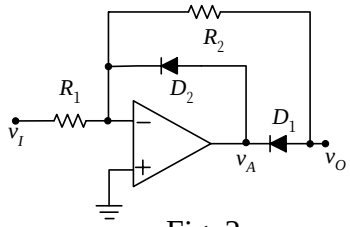

Fig. 2

(g) The phase of a negative feedback amplifier is -150º while its loop gain is 0 dB. Please indicate the amplifier's phase margin. (5%)

(h) Describe the Barkhausen criterion of oscillation. (5%)

(i) Please compare the transconductance g_m, output resistance r_o, intrinsic voltage gain A_0, input resistance R_i and power dissipation P_{diss} between BJT and FET. (5%)

(j) The circuit shown in Fig. 3 is a variation of class AB output stage. Please describe the purpose of Q_5 and R_{E1}. (5%)

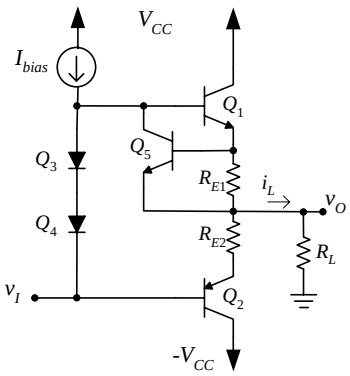

Fig. 3

2. For the circuit shown in Fig. 4, derive the relation between I_O and I_{REF} under finite current gain β and identical transistors. (5%)

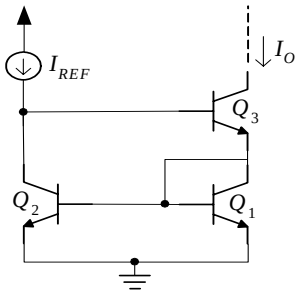

Fig. 4

3. Let the circuit shown in Fig. 5 under that the FET has V_t = 1V, $k_n'(W/L)$ = 1mA/V^2, V_{DD} = 5V, and R_D = 8KΩ.
   (a) What are the v_I and v_O values while the transistor operates just from cutoff region to saturation region? (5%)
   (b) What are the v_I and v_O values while the transistor just operates from saturation region to triode region? (5%)

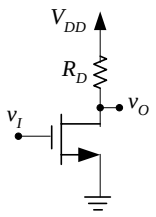

Fig. 5

4. The common-base amplifier shown in Fig. 6 under the following condition: I = 1mA, $\alpha \approx 1$, R_{sig} = 5KΩ, R_C = R_L =10KΩ. If the coupling capacitors C_1 and C_2 are ideal infinite.
   (a) Plot the small signal equivalent circuit for the circuit using T model. (5%)
   (b) Find voltage gain $A_v = v_o/v_i$, and (5%)
   (c) $R_{in.}$ (5%)
   (d) Describe the significant advantage and disadvantage of common-base amplifier in applications. (5%)

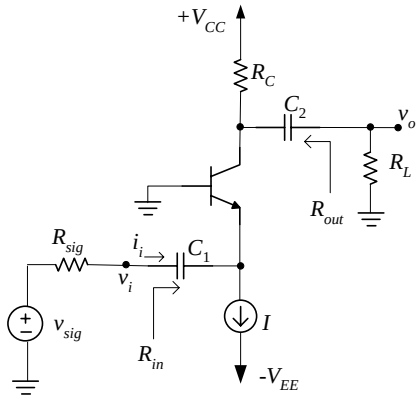

Fig. 6

5. The circuit shown in Fig. 7 is a waveform generator with ideal op amps.
   (a) Please plot the waveforms of $v_1(t)$ and $v_2(t)$. (5%)
   (b) If the op amps have output saturation voltages of ±10V and if a capacitor C = 0.01μF and a resistor R_1 = 1KΩ are used, find the values of R and R_2 such that the waveform v_1 has frequency 1KHz and 10V peak-to-peak amplitude. (10%)

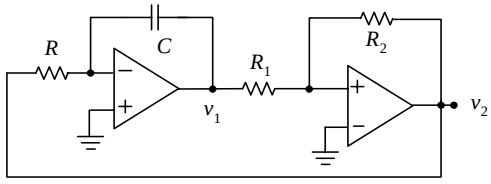

Fig. 7